ABSTRACT OF THE DISCLOSURE

A data reading apparatus, capable of reducing the recording field of a header portion, generates a read clock signal based on the average rotational speed and recording density of a disk. Delay circuits generate first and second delay clock signals of different phases. Three ID reading apparatuses operate in accordance with the read clock signal and the first and second delay clock signals to read address information at different timings. A selector circuit selects the best read address and error detection result from the read addresses and error detection results for the read addresses.